**Comparative analysis and optimization of active power and delay of 1-bit full adder at 45nm technology**

**Abstract**

An overview of performance analysis and compression between various parameters of a low power high speed conventional 1-bit full adder has been presented here. The work elucidated here gives a quantitative comparison of the adder cell performance. This paper shows the advancement over active power, leakage current and delay. The comparative study based on a new logic approach, which reduces power consumption. With power supply of 0.7V, we have achieved reduction in active power consumption of 98.28nW and propagation delay of 0.737ns,

which makes this circuit highly energy efficient. In this circuit we have reduced leakage current of 135.9nA. The designs have been carried out by virtuoso tool of cadence at 45nm technology.

**Tools:**

* DSch
* Microwind